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EXAMINER

CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/752,880

Applicant(s)

HAYCOCK ET AL.

Examiner

Thomas J. Cleary

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2004.
- 2a) ☒ This action is **FINAL**.      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-7, 9-11, 13-16, and 18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-7, 9-11, 13-16 and 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 101*

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 5, 9, 13, and 18 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The aforementioned claims include the limitation that the signals are transmitted by wireless communication. However, the independent claims from which the aforementioned claims respectively depend include the limitation that the signals are transmitted on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. A bus, by definition, is a set of hardware lines used for data transfer among the components of a computer system (See 'bus' in The Microsoft Computer Dictionary, 3<sup>rd</sup> Edition and 'bus' in The Free On-Line Dictionary of Computing). Wireless, by definition, is communications taking place without the use of interconnecting wires or cables (See 'wireless' in The Microsoft Computer Dictionary, 3<sup>rd</sup> Edition and 'wireless' in The Free On-Line Dictionary of Computing). Because the signals are transmitted on an SBD bus having ternary logic levels, the signals are transmitted on a set of hardware lines and therefore cannot be transmitted wirelessly. The device as claimed is inoperative as it claims a bus that is both constructed of hardware lines and is wireless.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5, 9, 13, and 18 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The aforementioned claims include the limitation that the signals are transmitted by wireless communication. However, the independent claims from which the aforementioned claims respectively depend include the limitation that the signals are transmitted on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. A bus, by definition, is a set of hardware lines used for data transfer among the components of a computer system (See 'bus' in The Microsoft Computer Dictionary, 3<sup>rd</sup> Edition and 'bus' in The Free On-Line Dictionary of Computing). Wireless, by definition, is communications taking place without the use of interconnecting wires or cables (See 'wireless' in The Microsoft Computer Dictionary, 3<sup>rd</sup> Edition and 'wireless' in The Free On-Line Dictionary of Computing). Because the signals are transmitted on an SBD bus having ternary logic levels, the signals are transmitted on a set of hardware lines and

therefore cannot be transmitted wirelessly. One of ordinary skill in the art would not have been able to construct a bus that is both constructed of hardware lines and is wireless.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-18 recite the limitation "a predetermined finite set of signals." The term "predetermined" as used in the aforementioned claims is indefinite because it does not indicate a criteria to be used for predetermination, nor does it indicate a manner of implementing the predetermination. Therefore, the scope of the claimed invention for the aforementioned claims cannot be reasonably determined by one having ordinary skill in the art.

7. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 10 recites the limitation "said busses" in Line 7. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 3, 6, 7, 10, 11, 14, 15, and 16 rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,601,196 to Dabral et al. ("Dabral")

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

10. In reference to Claim 1, Dabral discloses an apparatus comprising a buffer having at least one trigger, integrated on a component connected with a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), to observe and echo a

predetermined finites set of bi-direction signals transmitted on said memory bus (See Column 3 Lines 7-10).

11. In reference to Claim 2, Dabral discloses the limitations as applied to Claim 1 above. Dabral further discloses an observability port coupled with said buffer to receive said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), an observability bus connected with said observability port (See Figure 2 Numbers 291 and 292), and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).

12. In reference to Claim 3, Dabral discloses the limitations as applied to Claim 2 above. Dabral further discloses that said observability port is a logic observability port (See Column 3 Lines 10-14).

13. In reference to Claim 6, Dabral discloses a method comprising transmitting signals on a simultaneous bi-directions (SBD) memory bus having ternary logic level; a buffer having at least one trigger, integrated on a component connected with the bus (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), observing and echoing a predetermined finite set of signals transmitted on the bus (See Column 3 Lines 7-10).

14. In reference to Claim 7, Dabral discloses the limitations as applied to Claim 6 above. Dabral further discloses receiving said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10); and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).

15. In reference to Claim 10, Dabral discloses a memory (See Column 1 Lines 12-14); an input/output (I/O) port (See Column 1 Lines 12-14); and a microprocessor (See Column 1 Lines 12-14); a buffer means, integrated on a component coupled to one of the busses (See Figure 2 Number 250), for observing and echoing a predetermined finite set of signals transmitted on a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Column 1 Lines 12-14, Column 3 Lines 15-18, Column 3 Lines 7-10).

16. In reference to Claim 11, Dabral discloses the limitations as applied to Claim 10 above. Dabral further discloses means for receiving said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), and means for performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).



17. In reference to Claim 14, Dabral discloses a memory (See Column 1 Lines 12-14); an input/output (I/O) port (See Column 1 Lines 12-14); and a microprocessor (See Column 1 Lines 12-14); a buffer, having at least one trigger, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), for observing and echoing a predetermined finite set of bi-direction signals transmitted on said bus (See Column 3 Lines 7-10).

18. In reference to Claim 15, Dabral discloses the limitations as applied to Claim 14 above. Dabral further discloses an observability port coupled with said buffer to receive said echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), an observability bus connected with said observability port (See Figure 2 Numbers 291 and 292), and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14).

19. In reference to Claim 16, Dabral discloses the limitations as applied to Claim 15 above. Dabral further discloses that said observability port is a logic observability port (See Column 3 Lines 10-14).

***Claim Rejections - 35 USC § 103***

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claims 1, 2, 6, 7, 10, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,072,804 to Beyers, Jr. ("Beyers") in view of US Patent Number 5,933,594 to La Joie et al. ("La Joie"), US Patent Number 5,666,302 to Tanaka et al. ("Tanaka") and knowledge which is well known in the art.

22. In reference to Claim 1, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a buffer integrated on said component having at least one trigger, and connected with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to observe and echo a predetermined finite set of signals transmitted on said memory bus. La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing a predetermined finite set of signals by a monitoring system, which is equivalent to observing and echoing signals (See Column 2 Lines 34-41), from a bus. The Examiner takes Official Notice that a memory bus is a common

component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

23. In reference to Claim 2, Beyers, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 1 above. Beyers further teaches an observability bus, connected between a port on the analyzer buffer, which is equivalent to the observability port (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control, which is equivalent to the logic analyzer and bus analyzer (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in

the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 2, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

24. In reference to Claim 6, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach transmitting signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels; a buffer, integrated on said component, having at least one trigger; and connected with the bus, observing and echoing a predetermined finite set of the signals transmitted on the bus. La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing a predetermined finite set of signals by a monitoring system, which is equivalent to observing and echoing signals (See Column 2 Lines 34-41) from the bus. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at

the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 6, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

25. In reference to Claim 7, Beyers, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 6 above. Beyers further teaches receiving the signals (See Column 13 Lines 34-36); capturing the signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 7, in order to monitor the individual components as well as identify and diagnose

errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

26. In reference to Claim 10, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a memory; an I/O port; and a microprocessor; and a buffer means, integrated on a component coupled to one of the busses, for observing and echoing a predetermined finite set of signals transmitted on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. La Joie teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1 Number 12); and a buffer (See Figure 1 Number 20) that stores data captured from the bus, which is equivalent to observing and echoing signals (See Column 14 Lines 1-13). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of

La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 10, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

27. In reference to Claim 11, Beyers, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied Claim 10 above. Beyers further teaches receiving the signals (See Column 13 Lines 34-36); capturing the signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 11, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

28. In reference to Claim 14, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a memory; an I/O port; a microprocessor; and a buffer means, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to observe and echo a predetermined finite set of bi-direction signals transmitted on said bus. La Joie teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1 Number 12); and a buffer having a trigger (See Figure 1 Number 20) that stores data captured from the bus, which is equivalent to observing and echoing signals (See Column 14 Lines 1-13). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 14, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the



number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

29. In reference to Claim 15, Beyers, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 14 above. Beyers further teaches an observability bus, connected between a port on the analyzer buffer, which is equivalent to the observability port (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control, which is equivalent to the logic analyzer and bus analyzer (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers with the bus monitoring system of La Joie and the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 15, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie) and to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

30. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers, La Joie, Tanaka, and knowledge commonly known in the art as applied to Claims 2 and 15 above, and further in view of US Patent Number 6,496,583 to Nakamura et al. ("Nakamura").

31. In reference to Claim 3, Beyers, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 2 above. Beyers, La Joie, and Tanaka do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers, La Joie, and Tanaka with the device of Nakamura, resulting in the invention of Claim 3, in order to provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

32. In reference to Claim 16, Beyers, La Joie, Tanaka, and knowledge commonly known in the art teach the limitations as applied to Claim 15 above. Beyers, La Joie, and Tanaka do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Beyers, La Joie, and Tanaka with the device of Nakamura, resulting in the invention of Claim 16, in order to provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

33. Claims 1, 6, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,488,688 to Gonzales et al. ("Gonzales"), Tanaka, and knowledge commonly known in the art.

34. In reference to Claim 1, Gonzales teaches a buffer having at least one trigger (See Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 1 and Column 2 Lines 23-26), to observe and echo a predetermined finite set of signals transmitted on said bus (See Column 2 Lines 23-26). Gonzales does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

35. In reference to Claim 6, Gonzales teaches a buffer having at least one trigger (See Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 1 and Column 2 Lines 23-26), observing and echoing a predetermined finite set of signals transmitted on the bus (See Column 2 Lines 23-26. Gonzales does not teach transmitting the signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 6, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

36. In reference to Claim 10, Gonzales inherently includes a memory and an I/O port. Gonzalez teaches a microprocessor (See Figure 1 Number 21); and a buffer means, integrated on a component coupled to a bus (See Figure 1 and Column 2 Lines 23-26), for observing and echoing a predetermined finite set of signals transmitted on a bus (See Figure 1 and Column 2 Lines 23-26). Gonzales does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 10, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

37. In reference to Claim 14, Gonzales inherently includes a memory and an I/O port. Gonzalez teaches a microprocessor (See Figure 1 Number 21); and a buffer, having at least one trigger (See Column 2 Lines 23-26), integrated on a component coupled with a bus (See Figure 1 and Column 2 Lines 23-26), to observe and echo a predetermined

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finite set of signals transmitted on a bus (See Figure 1 and Column 2 Lines 23-26).

Gonzales does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Gonzales with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 14, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

38. Claims 1, 6, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,903,719 to Yamamoto ("Yamamoto"), Tanaka, and knowledge commonly known in the art.

39. In reference to Claim 1, Yamamoto teaches a buffer having at least one trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 2 and Column 2 Lines 3-5), to observe and echo a predetermined finite set of signals transmitted on said bus (See Column 2 Lines 35-44).

Yamamoto does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

40. In reference to Claim 6, Yamamoto teaches a buffer having at least one trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 2 and Column 2 Lines 3-5), observing and echoing a predetermined finite set of signals transmitted on the bus (See Column 2 Lines 35-44). Yamamoto does not transmitting signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 6, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

41. In reference to Claim 10, Yamamoto teaches a memory (See Figure 2 Number 12); an I/O port (See Figure 2 Number 17); and a microprocessor (See Figure 2 Number 11); and a buffer means, integrated on a component coupled to a bus (See Figure 2 and Column 2 Lines 3-5), for observing and echoing a predetermined finite set of signals transmitted on the bus (See Column 2 Lines 35-44). Yamamoto does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 10, in order to reduce the



number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

42. In reference to Claim 14, Yamamoto teaches a memory (See Figure 2 Number 12); an I/O port (See Figure 2 Number 17); and a microprocessor (See Figure 2 Number 11); and a buffer, having at least one trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component coupled with a bus (See Figure 2 and Column 2 Lines 3-5), to observe and echo a predetermined finite set of signals transmitted on a bus (See Column 2 Lines 35-44). Yamamoto does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Yamamoto with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 14, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

43. Claims 1, 6, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,119,254 to Assouad et al. ("Assouad"), Tanaka, and knowledge commonly known in the art.

44. In reference to Claim 1, Assouad teaches a buffer having at least one trigger (See Column 7 Lines 43-46), integrated on a component connected with a bus (See Figure 3 Numbers 104 and 105), to observe and echo a predetermined finite set of signals transmitted on said bus (See Column 7 Lines 50-62). Assouad does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 1, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

45. In reference to Claim 6, Assouad teaches a buffer having at least one trigger (See Column 7 Lines 43-46), integrated on a component connected with a bus (See Figure 3 Numbers 104 and 105), observing and echoing a predetermined finite set of signals transmitted on the bus (See Column 7 Lines 50-62. Assouad does not teach transmitting signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 6, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

46. In reference to Claim 10, Assouad teaches a memory (See Figure 3 Number 112); an I/O port (See Figure 3 Number 204); and a microprocessor (See Figure 3 Number 111); and a buffer means, integrated on a component coupled to a bus (See Figure 3 Numbers 104 and 105), for observing and echoing a predetermined finite set of signals transmitted on a bus (See Column 7 Lines 50-62). Assouad does not teach that

the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus"). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

47. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 10, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

48. In reference to Claim 14, Assouad teaches a memory (See Figure 3 Number 112); an I/O port (See Figure 3 Number 204); and a microprocessor (See Figure 3 Number 111); and a buffer, having at least one trigger (See Column 7 Lines 43-46), integrated on a component coupled to a bus (See Figure 3 Numbers 104 and 105), to observe and echo a predetermined finite set of signals transmitted on a bus (See Column 7 Lines 50-62). Assouad does not teach that the bus is a simultaneous bi-directional (SBD) memory bus having ternary logic levels. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The

Memory Bus”). Tanaka teaches a simultaneous bi-directional bus having ternary logic levels (See Abstract, Figure 1, and Column 1 Lines 9-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Assouad with the simultaneous bi-directional bus of Tanaka, resulting in the invention of Claim 16, in order to reduce the number of necessary transmission lines while maintaining the same transmission rate (See Column 1 Lines 16-26 of Tanaka).

### ***Claim Objections***

49. Claims 10, 11, and 13 are objected to because of the following informalities: In Line 9 of Claim 10, the word “bus” appears to have been erroneously included in the phrase “...bus simultaneous bi-directional (SBD)...”. Appropriate correction, if necessary, is required.

### ***Response to Arguments***

50. Applicant's arguments filed 14 July 2004 with respect to Claims 1-18 have been fully considered but are moot in view of the new ground(s) of rejection. Applicant has modified the scope of the claims to include “a simultaneous bi-directional (SBD) bus having ternary logic levels” and “bi-direction signals”. As shown above, such changes are not persuasive to overcome a rejection based on 35 USC §§102 and 103. The new

ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

### ***Conclusion***

51. The following art made of record and not relied upon is considered pertinent to applicant's disclosure: US Patent Number 6,781,406 to Emberling et al.

52. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-


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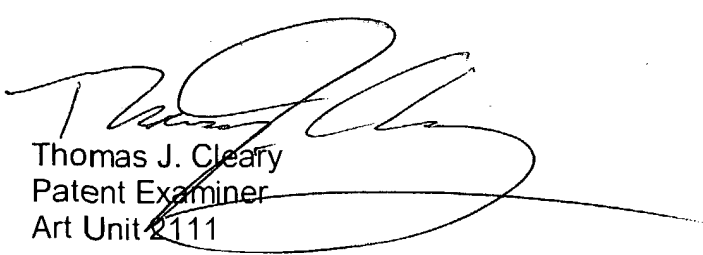
5824. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Beginning November 2004, the Examiner's telephone number will be changing to 571-272-3624, and the Examiner's supervisor's telephone number will be changing to 571-272-3632.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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